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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/730,108	12/09/2003	Toshio Miyazawa	520.40848CX1	2691

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EXAMINER

AWAD, AMR A

ART UNIT

PAPER NUMBER

2675

DATE MAILED: 09/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/730,108	Applicant(s) MIYAZAWA ET AL.	
	Examiner Amr Awad	Art Unit 2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 December 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-42 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-42 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>3/5/2004</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Information Disclosure Statement

1. The Examiner has considered the information disclosure statement filed 3/5/2004; see attached PTO-1449.

Priority

2. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. 09/988,209, filed on 11/19/2001.

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claims 1-42 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-36 of U.S. Patent No. 6,686,899 (Pat-899). Although the conflicting claims are not identical, they are not

patentably distinct from each other because the claims of the present application are substantially similar to claims 1-36 of Pat-899. For example, by comparing claim 1 of the present application to claim 1 of Pat-899, we can see that the preamble "a display device including a plurality of pixels and a driver circuit..." of the present application is equivalent to the preamble "a display device including a pair of substrates... a plurality of pixels formed between said pair of substrates..." of Pat-899. The limitation "a pair of a first NMISTFT..." of the present application is similar to the limitation "a pair of a first NMISTFT..." of pat-899. The limitation "each of said first NMISTFT and said first PMISTFT..." of the present application is similar to the limitation "each of said first NMISTFT and said first PMISTFT..." of pat-899. Similarly with respect to the rest of the limitations of claim 1, we can see that the limitations are substantially similar. The minor difference between the two claims is that the preamble in the present application does not recite having a pair of substrates. It is inherent that such display type described in claim 1 of the present application would include a pair of substrates. For example claims 2-3 of the present application are almost identical to claims 2 and 4 of Pat-899. Also claim 5 of the present application is substantially similar to claim 9 of Pat-899. Similarly with respect of the claims, we can see that there is very little difference, and such differences would have been obvious to a person of ordinary skill in the art or inherent such as the recitation of the pair of substrates.

Allowable Subject Matter

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5. Claims 1-42 would be allowed if a terminal disclaimer is filed to overcome the obvious double patent rejection.

6. The following is an examiner's statement of reasons for allowance:

None of the cited art either singularly or in combination teaches or fairly suggests a display device with a level converter circuit that includes the configuration described in any one of the independent claims. For example, Kubota et al. (US patent NO.

6,580,411) in figure 2 shows a pair of first transistors (M13 & M15) and a pair of second transistors (M14 & M17) configured approximately similar to Fig. 1A of the present invention wherein each pair of transistors of the first pair (NMOS1 & PMOS1) and the second pair (NMOS2 & PMOS1) are connected back-to-back. Matsuzaki et al. (US patent NO. 6,307,236) in figures 9 and 19 shows the back-to-back configuration.

However, the cited references do not teach or suggest having the first and second having the configuration and the connection disclosed in independent claims 1 and 5 (lines 10-19 of claim 1, and lines 11-20 of claim 5). With respect to independent claims 10, 12 and 14, Hirano (US patent NO. 5,650,742) in figure 1 shows first, second and third transistor (Qn101, Qn102 and Qp102) configured approximately similar to Fig. 10A of the present invention wherein a first, second and third transistor (NMOS1, NMOS2 and NMOS3) are connected according to the configuration disclosed in claims 10, 12 and 14. However, none of the cited art teaches or fairly suggests the exact connections of the first MISTFT, second MISTFT and third MISTFT as disclosed in independent

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claims 10, 12 and 14 (lines 11-20 of claim 10, 11-19 of claim 12 and lines 13-23 of claim 14).

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Amr Awad whose telephone number is (703)308-8485. The examiner can normally be reached on Monday through Friday from 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Razavi can be reached on (703)305-4713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A.A



AMR A. AWAD
PRIMARY EXAMINER